Factsheet

IEEE 1394® - SI16FW10

Silicon Cores™

Core to the Intelligent System™

Link Layer Controller

***Silicon Interfaces'* Link core is a functional block available for insertion into a customer's ASIC design, which supports the IEEE 1394-1995 Draft specifications for a high-speed serial bus. The *SI16FW10* Link core is implemented using VHDL synthesizable code to provide portability across *Silicon Interfaces'* Gate Array and Cell-Based ASIC technologies**

The SI16FW10, 1394 Link Layer Controller Core provides data packet delivery service for asynchronous and isochronous (real-time) data transmission. It performs arbitration request, packet generation and checking as well as data and acknowledgement transmission. Packet generation includes the header, address, 32-bit CRC data, packet channel, and destination address and transaction code. *Silicon Interfaces'* link layer controller core also provides complete support for bus Cycle Master and cycle control operation. SI16FW10 is designed to support 100, 200 and 400 Mbps transmission, when used with the appropriate external physical layer device. This is depending on speed provided with a 2-bit, 4-bit or 8-bit interface, which does not require special high-speed buffers.

The SI16FW10 highly integrated single-chip core is *Silicon Interfaces'* intellectual property and represents our proven Link Layer design experience, expertise in complex design. The complete modular design of the core facilitates easy customization to include value added and distinguishing features.

Product Specifications

- Fully synthesizable Register Transfer Level (RTL) VHDL core.
- Test Bench Environment: Verilog
- Targeted FPGA Xilinx Spartan-6 / Virtex-6
- Clock Frequency: 50 MHz

Options:

(May be separately priced)

Adaptations:

√ 32-bit PCI host interface possible.

Add-ons:

√ NIL.

Product Highlights

- ☑ Fully compliant with IEEE 1394-1995 Standards.
- ☑ Half Duplex Independent; Transmit and Receive Data Path controlled by Rx Tx Controller.
- ☑ **32-bit Generic Host Bus Interface.**
- ☑ **Has a hand-shaking signal for Host.**
- ☑ Full Implementation of Link Core.
- ☑ Supports Asynchronous, Isochronous and Cycle start packet Transmit and Receive.
- ☑ **Automatic 32-bit CRC generation and error detection. CRC**
- ☑ **Cycle** Master cable.
- ☑ **Supports all required 11 Packet Formats; 9 Asynchronous and 2 Isochronous as per standard.**
- ☑ **2 Kbytes Transmit and Receive FIFO or Buffer.**
- ☑ **PHY Link Interface conforms to the specifications described in the Annex J of the IEEE 1394-1995 standard.**
- ☑ **Supports** 100/200 and 400 Mbps bus rates.
- ☑ Single clock domain throughout the system.

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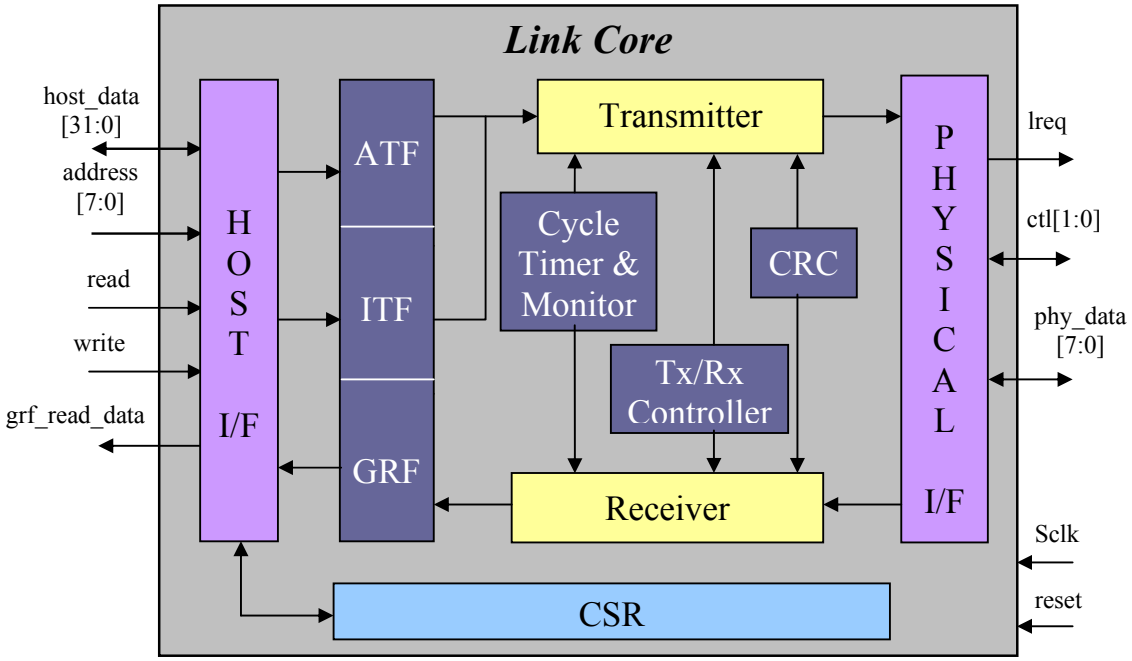
LLC Block Representative Schematic:



Host Interface: The Host Interface allows the SI16FW10 to be easily connected to the most 32-bit host processors. The host interface consists of a 32-bit data bus and an 8-bit address bus.

Physical Interface: The Physical (phy) Interface provides phy-level services to the transmitter and receiver. This includes gaining access to the serial bus, sending packets, receiving packets, and sending and receiving acknowledge packets.

Control and Status Register: The Control and Status Register store the vital information desirable for the proper working of the core.

Transmit and Receive FIFOs: The SI16FW10 contains two transmit FIFOs i.e. ATF (asynchronous transmit FIFO) and ITF (isochronous transmit FIFO) and one receive FIFO i.e. GRF (general receive FIFO).

Transmitter: The transmitter retrieves data from either the ATF or the ITF and creates correctly formatted serial-bus packets to be transmitted through the phy interface.

Receiver: The receiver takes the incoming data from the phy interface, checks the validity and stores the valid data into the receive memory or stores the status of the received corrupt packet into the CSR.

Cycle Timer and Monitor: Each node with isochronous data-transfer capability has a cycle-time register as defined in the IEE1394-1995 standard. The Cycle Timer contains a cycle-time register, which provides the fields, which specify the current time value. The cycle monitor observes chip activity and handles scheduling of isochronous activity.

Tx/Rx Controller: The Tx/Rx controller generates signals for controlling the transmit and receive operations.

CRC: The CRC module generates the cyclic redundancy check value for error detection of packets to be transmitted and received.

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